AMENDMENTS TO THE SPECIFICATION

Please amend the specification beginning at page 8, line 7 as follows:

An IGBT 6 has a second emitter for detecting a collector current Ic. A voltage generated at a resistor 23 inserted in series to the second emitter circuit is entered into a positive input terminal of a comparator 24. A reference voltage source 25 is connected to a negative input terminal of the comparator 24, and an output of the comparator 24 is entered into a D terminal of a latch circuit ~~26~~ 27. Then, ~~an output from a Q terminal of the latch circuit 26 is entered into a D terminal of a latch circuit 27. The~~ the output of the aforementioned comparator 9 as a carry signal is entered into a C terminal of the latch circuit ~~26~~ 27 through an inverter 28, and concurrently entered into a C terminal of the latch circuit 27 through an inverter 28.

Please amend the specification beginning at page 8, line 21 as follows:

The operation of the above circuit will be described with reference to the time chart in FIG. 4. The comparator 24 determines whether the collector current Ic flowing through the IGBT 1 turned on when an input signal VIN of a (n – 1)-th pulse is an ON signal of Low Level is greater than one-half of a rated current, and then supplies the determination result to the latch circuit ~~26~~ 27.

Please amend the specification beginning at page 9, line 1 as follows:

During the course that the (n – 1)-th pulse input signal VIN changes from the ON signal of Low Level to an OFF signal (a signal for turning off the IGBT 6) of High Level,

upon rising beyond an input-OFF threshold (at Time T3), the comparator 9 outputs the High Level signal. In response to this signal, the signal supplied to the latch circuit 27 (judgment result) is latched by the latch circuit 27 and that signal is outputted from a Q terminal of ~~latched by the latch circuit 26 is supplied to~~ the latch circuit 27.